WHAT IS CLAIMED IS:

1. A cache system, comprising:

a first bus;

a second bus;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section and output data read from said memory section to said first bus;

a cache memory;

instruction means for outputting to said second bus a command for instruction to write back data of said cache memory into said main memory; and

a cache memory control section including a directory section for storing information regarding an address of said main memory of data stored in said cache memory and a reset terminal to which a first reset signal is inputted such that, when the first reset signal is asserted, at least an element of said cache memory control section which takes part in control of said first bus except said directory section is reset, said cache memory control section performing reading and writing of data between said main memory and said cache memory over said first bus, said cache memory control section

performing write back processing of the data of said cache memory into said main memory in accordance with the command inputted over said second bus.

2. A cache system, comprising:

a first bus;

a second bus;

a third bus;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section and output data read from said memory section to said first bus;

a cache memory;

instruction means for outputting to said second bus a command for instruction to write back data of said cache memory into said main memory;

a cache memory control section for performing reading and writing of data between said main memory and said cache memory over said first bus and performing write back processing of the data of said cache memory into said main memory in accordance with the command inputted over said second bus;

an interface section for interfacing between said first bus and said third bus; and

an isolate section interposed between an output side of said interface section and said first bus for isolating said output side of said interface section and said first bus from each other when a control signal inputted to a control terminal becomes valid.

3. A cache system, comprising:

a first bus;

a second bus;

a signal line different from said first bus;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section, output data read from said memory section to said first bus, and receive data and an address from said signal line and write the data and the address into said memory section;

a cache memory;

instruction means for outputting to said second bus a command for instruction to write back data of said cache memory into said main memory; and

a cache memory control section for performing reading and writing of data between said main memory and said cache memory over said first bus and outputting data and an address of said cache memory to said signal line

in accordance with the command inputted over said second bus thereby to perform write back processing into said main memory.

4. A dual system which comprises a first system and a second system one of which is operated in an act state while the other is operated in a standby state, and a memory confounding line and a system confounding line for interconnecting said first system and said second system, each of said first system and said second system including:

a first bus;

a second bus;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section, output data read from said memory section to said first bus, and receive data of the other system which is in the act state over said memory confounding line and write the data into said memory section;

a cache memory;

instruction means for outputting to said second bus a first command for instruction to write back data of said cache memory into said main memory; and

a cache memory control section including a

directory section for storing information regarding an address of said main memory of data stored in said cache memory and a first reset terminal to which a first reset signal is inputted such that, when the first reset signal is asserted, at least an element of said cache memory control section which takes part in control of said first bus except said directory section is reset, said cache memory control section performing reading and writing of data between said main memory and said cache memory over said first bus, said cache memory control section performing write back processing of the data of said cache memory into said main memory in accordance with the first command inputted over said second bus.

5. A dual system according to claim 4, wherein each of said first system and said second system further includes a system control section for controlling state changeover between the act state and the standby state over said system confounding line, and said system control section controls so that the first command is outputted after the first reset signal is asserted upon state changeover from the act state to the standby state.

6. A dual system according to claim 5, wherein an element of said cache memory control section which takes part in control of said second bus is reset in response

to the first reset signal.

7. A dual system according to claim 5, wherein said main memory includes a second reset terminal to which a second reset signal is inputted such that, when the second reset signal is asserted, at least an element of said main memory which takes part in control of said first bus is reset, and said cache memory control section controls such that the first command is outputted after the second reset signal is asserted upon state changeover from the act state to the standby state.

8. A dual system which comprises a first system and a second system one of which is operated in an act state while the other is operated in a standby state, and a memory confounding line and a system confounding line for interconnecting said first system and said second system, each of said first system and said second system including:

a first bus;

a second bus;

a third bus;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section, output data read from said memory section to said first

bus, and receive data of the other system which is in the act state over said memory confounding line and write the data into said memory section;

a cache memory;

instruction means for outputting to said second bus a first command for instruction to write back data of said cache memory into said main memory;

a cache memory control section for performing reading and writing of data between said main memory and said cache memory over said first bus and performing write back processing of the data of said cache memory into said main memory in accordance with the first command inputted over said second bus;

an interface section for interfacing between said first bus and said third bus; and

a first isolate section interposed between an output side of said interface section and said first bus for isolating said output side of said interface section and said first bus from each other when a first control signal inputted to a first control terminal becomes valid.

9. A dual system according to claim 8, wherein each of said first system and said second system further includes a system control section for controlling state changeover between the act state and the standby state

over said system confounding line, and said system control section controls so that the first command is outputted after the first control signal becomes valid upon state changeover from the act state to the standby state.

10. A dual system according to claim 9, wherein each of said first system and said second system further includes a second isolate section interposed between an output side of said system control section and said first bus for isolating said output side of said system control section and said first bus when a second control signal inputted to a second control terminal becomes valid, and said system control section controls so that the first command is outputted after the first and second control signals become valid upon state changeover from the act state to the standby state.

11. A dual system which comprises a first system and a second system one of which is operated in an act state while the other is operated in a standby state, and a memory confounding line and a system confounding line for interconnecting said first system and said second system, each of said first system and said second system including:

a first bus;

a second bus;

a first signal line;

a main memory having a memory section for storing data, said main memory being operable to write data inputted from said first bus into said memory section, output data read from said memory section to said first bus, receive data and an address from said first signal line and write the data and the address into said memory section, and receive data of the other system which is in the act state from said memory confounding line and write the data into said memory section;

a cache memory;

instruction means for outputting to said second bus a first command for instruction to write back data of said cache memory into said main memory; and

a cache memory control section for performing reading and writing of data between said main memory and said cache memory over said first bus and outputting data and an address of said cache memory to said first signal line in accordance with the first command inputted over said second bus thereby to perform write back processing into said main memory.

12. A dual system according to claim 11, wherein each of said first system and said second system further

includes a system control section for controlling state changeover between the act state and the standby state over said system confounding line, and said system control section controls so that the first command is outputted upon state changeover from the act state to the standby state.

13. A dual system according to claim 12, wherein each of said first system and said second system further includes a second signal line for interconnecting said main memory and said system control section, said cache memory control section notifying completion of the write back processing using said first signal line when the write back processing is completed, said main memory asserting said second signal line when the notification is received over said first signal line, said system control section which is in the system in the act state instructing the other system to change over the state from the standby state to the act state over said system confounding line when said second signal line is asserted.

14. A dual system according to claim 13, wherein, when the notification is received over said first signal line, said main memory writes information representative of completion of the write back processing into a particular address area of said memory section.

15. A dual system according to claim 13, wherein said main memory includes a register and writes, when the notification is received over said first signal line, information representative of completion of the write back processing into said register.

16. A dual system according to claim 5, wherein each of said first system and said second system further includes a first signal line for interconnecting said cache memory control section and said system control section, said cache memory control section which is in the system in the act state asserting said first signal line when the write back processing is completed, said system control section which is in the system in the act state instructing the other system to change over the state from the standby state to the act state over said system confounding line when said first signal line is asserted.

17. A dual system according to claim 16, wherein, when said first signal line is asserted, said main memory writes information representative of completion of the write back processing into a particular address area of said memory section.

18. A dual system according to claim 16, wherein said main memory includes a register and writes, when said

first signal line is asserted, information representative of completion of the write back processing into said register.

19. A dual system according to claim 9, wherein said system control section includes a first timer for being periodically reset by said instruction means and outputting a first timeout signal when said first timer measures a first predetermined time and a second timer for measuring a second predetermined time which is not shorter than a time required until said cache memory control section ends the write back processing after the first timeout signal is outputted, and said system control section performs the interrupt notification based on the first timeout signal and instructs, when said first signal line is not asserted, the other system to change over the state from the standby state to the act state over said system confounding line based on the second timeout signal.

20. A dual system according to claim 14, wherein one of said first and second systems whose state has been changed over from the standby state to the act state reads the information from the particular address area and executes, when the information indicates completion of the write back processing, based on the data stored in

said main memory, but loads, when the information does not indicate completion of the write back processing, a program into said memory and then executes the program.

21. A dual system according to claim 15, wherein one of said first and second systems whose state has been changed over from the standby state to the act state reads the information from said register of the other system and executes, when the information indicates completion of the write back processing, based on the data stored in said main memory, but loads, when the information does not indicate completion of the write back processing, a program into said memory and then executes the program.

22. A dual system according to claim 9, wherein each of said first system and said second system further includes a first signal line for interconnecting said cache memory control section and said main memory and a second signal line for interconnecting said main memory and said system control section, said cache memory control section which is in the system in the act state asserting said first signal line when the write back processing is completed, said main memory which is in the system in the active state asserting said second signal line when said first signal line is asserted, said system

control section which is in the system in the act state instructing the other system to change over the state from the standby state to the act state over said system confounding line when said second signal line is asserted.

23. A dual system according to claim 12, wherein said cache memory control section which is in the system in the act state outputs, when the write back processing is completed, a second command representative of completion of the write back processing to said first bus, and said system control section which is in the system in the act state instructs the other system to change over the state from the standby state to the act state over said system confounding line based on the second command.

24. A dual system according to claim 5, wherein each of said first system and said second system further includes a first signal line for interconnecting said main memory and said system control section, said cache memory control section which is in the system in the act state outputting a second command representative of completion of the write back processing to said first bus when the write back processing is completed, said main memory which is in the system in the act state asserting said first signal line based on the second command, said system control section which is in the system in the act

state instructing the other system to change over the state from the standby state to the act state over said system confounding line when said first signal line is asserted.

25. A dual system according to claim 12, wherein each of said first system and said second system further includes a second signal line for interconnecting said main memory and said system control section, said cache memory control section which is in the system in the act state outputting a second command representative of completion of the write back processing to said first bus when the write back processing is completed, said main memory which is in the system in the act state asserting said second signal line based on the second command, said system control section which is in the system in the act state instructing the other system to change over the state from the standby state to the act state over said system confounding line when said second signal line is asserted.